Dolphin Technology

# DOLPHIN TECHNOLOGY PRODUCT OFFERING
# DDR PHY DDR CONTROLLER

## DDR PHY & DDR CONTROLLER

Dolphin Technology's hardened DDR4/3/2 SDRAM PHY and LPDDR3/2 SDRAM PHY IP is a silicon-proven, Combo PHY supporting speeds up to 3200 Mbps. It is fully compliant with the DFI 3.1 specification, and features include slew rate control, per-bit de-skew, gate training, read and write leveling and built-in self test (BIST).

In addition, our PHY IP is optimized to provide a complete solution when combined with Dolphin's DDRx and LPDDRx SDRAM Memory Controller IP.

| DDR PHY (HARD IP) | 16nm FF+ FFC | 28nm HP, HPx LP, ULP | 40nm G, LP ULP | 55nm GP, LP ULP, EF | 65nm GP LP | 80nm G GC | 90nm G, GT EF |
|---|---|---|---|---|---|---|---|
| DDR4/3/2 PHY (DFI 3.1 compliant) | ● | ● | ● | | | | |
| LPDDR3/2 PHY (DFI 3.1 compliant) | ● | ● | ● | | | | |
| DDR3/2 PHY (DFI 3.1 compliant) | | | ● | ● | ● | | |
| Maximum speed, with 1.8V oxide (Mbps) | 3200 | 3200 | 2133 | 1600 | 1600 | | |
| Maximum speed, with 2.5V oxide (Mbps) | 1600 | 1600 | 1600 | 1600 | 1600 | | |
| IP is split into two hard macros (one for commands, control and address pins, one for 8-bit data bus) | ● | ● | ● | ● | ● | | |
| Supports custom number of address bits | ● | ● | ● | ● | ● | | |
| Compensation controller and pads for automatic driver and receiver termination impedance calibration | ● | ● | ● | ● | ● | | |
| Slew rate control, per-bit de-skew, gate training, read and write leveling | ● | ● | ● | ● | ● | | |
| JTAG signals for Mentor/Synopsys and LogicVision | ● | ● | ● | ● | ● | | |
| BIST with Pseudo Random Pattern Generator | ● | ● | ● | ● | ● | | |
| Scannable flops | ● | ● | ● | ● | ● | | |
| Wirebond, flip-chip and cup configurations | ● | ● | ● | ● | ● | | |

## DDR CONTROLLER (SOFT IP)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DFI 3.1 Interface with Matching or 1:2 Frequency Ratio | ● | ● | ● | ● | ● | ● | ● |
| Built-in Gate Training and Read/Write Leveling | ● | ● | ● | ● | ● | ● | ● |
| Maximum speed (Mbps) | 3200 | 3200 | 2133 | 1600 | 1600 | 1600 | 1600 |
| JEDEC Standard DDR4/3/2 and LPDDR3/2 SDRAM | ● | ● | ● | | | | |
| JEDEC Standard DDR3/2 and LPDDR2 SDRAM | | | | ● | ● | ● | ● |
| Multi-port configurable AXI4 interface w/QoS signaling | ● | ● | ● | ● | ● | ● | ● |
| Multi-port arbitration engine with programmable dynamic priority algorithm | ● | ● | ● | ● | ● | ● | ● |
| Pipeline option for frequency vs. latency tradeoff | ● | ● | ● | ● | ● | ● | ● |
| Fully configurable for various performances and requirements | ● | ● | ● | ● | ● | ● | ● |
| FPGA portable (Xilinx PHY & Altera PHY compatible) | ● | ● | ● | ● | ● | ● | ● |
| BFM verification suite | ● | ● | ● | ● | ● | ● | ● |
| Single AXI4-Lite programming interface | ● | ● | ● | ● | ● | ● | ● |
| AXI4 dynamic QoS signaling for non-blocking communications | ● | ● | ● | ● | ● | ● | ● |
| Support for low-latency bypass ports/channels | ● | ● | ● | ● | ● | ● | ● |
| Advanced dynamic QoS support based on Queuing Theory and Traffic Hysteresis | ● | ● | ● | ● | ● | ● | ● |

**Front End views are available under NDA. For more information, contact: sales@dolphin-ic.com**

Dolphin Technology, Inc. 333 W Santa Clara Street, Suite 920 San Jose, CA 95113
www.dolphin-ic.com Tel: +1 (408) 392-0012 Fax: +1 (408) 392-0090