

DOLPHIN TECHNOLOGY PRODUCT OFFERING

I/O

16nm

28nm

40nm

Dolphin Technology offers an extensive array of Interface IP, all of which has been optimized for ultra high performance across all processes supported. Our I/O portfolio includes: Standard I/O (General Purpose I/O or GPIO), Specialty I/O (bus-specific I/O), NAND Flash I/O and DDRx & LPDDRx I/O.

We specialize in Staggered, Inline and Flip Chip pads with aggressive pitch for the most demanding designs, whether pad or core limited. Plus, our I/O Compiler enables us to customize the entire library based on process-specific and chip-specific options.

65nm

80nm

90nm

55nm

	FF+	HP, HPx	G, LP	GC, LP	GP	G	G, GT
GENERAL PURPOSE I/O	FFC	LP, ULP	ULP	ULP, EF	LP	GC	EF
I/O drive strengths 2/4/6/8/10/12 mA	•	•	•	•	•	•	•
1.8V Xtrs, 1.8V output drive/3.3V Tolerant	•						
1.8V Xtrs, 1.8V/3.3V output drive Capable	•			_			
1.8V Xtrs, 1.8V output drive/2.5V/3.3V Tolerant		•	•	•	•	•	•
1.8V Xtrs, 1.8V/2.5V/3.3V output drive Capable		•	•	•	•	•	•
2.5V Xtrs, 2.5V output drive/3.3V Tolerant		•	•	•	•	•	•
2.5V Xtrs, 2.5V/3.3V output drive Capable						•	
DDR I/O							
Configurable single-ended and differential I/O's	•	•	•	•	•	•	•
DDR4/3/2 & LPDDR3/2 I/O with PVT Compensation and	•	•					
PVT compensated internal termination RTT using 1.8V Xtrs							
DDR4/3/2 & LPDDR3/2 I/O with PVT Compensation and		•					
PVT compensated internal termination RTT using 2.5V Xtrs DDR3/2/1 & LPDDR2/1 I/O with PVT Compensation and							
PVT compensated internal termination RTT using 1.8V Xtrs			•	•	•	•	•
DDR3/2/1 & LPDDR2/1 I/O with PVT Compensation and							
PVT compensated internal termination RTT using 2.5V Xtrs			•	•	•	•	•
NAND FLASH I/O				_		T	T
ONFI 4/3/2/1 and Toggle 2/1 NAND compliant	•	•	•	•	•		
Configurable single-ended and differential I/O's	•	•	•	•	•		
NAND Flash I/O with PVT Compensation and PVT	•	•	•	•	•		
compensated internal termination RTT using 1.8V Xtrs							
Drive capability up to 80pF	•	•	•	•	•		
SPECIAL PURPOSE I/O							
LVPECL I/O with PVT Compensation	•	•	•	•	•	•	•
LVDS/LVPECL Combo with PVT Compensation	•	•	•	•	•	•	•
PCI	•	•	•	•	•	•	•
12C	•	•	•	•	•	•	•
I/O FEATURES						1	
Libraries include configurable I/O's, power cells, fillers,	•	•	•	•	•	•	•
spacers, and analog or calibration cells	•						
Pad design with 25um pitch	•	•	•	•	•	•	•
Supports wirebond/CUP and flipchip packages		-		•	•	•	•
Programmable metal stack options	•	•	•	•	•	•	•
4 different slew rate options	•	•	•	•	•	•	•
Built-in JTAG Logic for testability	•	•	•	•	•	•	•
Input/Output registers options	•	•	•	•	•	•	•
Bus-hold(sustain) and pull-up/pull-down options	•	•	•	•	•	•	•
Built-in ESD and Latchup Prevention circuits	•	•	•	•	•	•	•