Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
eMMC / SD / SDIO

eMMC/SD/SDIO - PHY (HARD IP)

Dolphin Technology's hardened eMMC5.1/SD4.1/SDIO4.1 HS400 PHY IP provides a complete physical interface between Dolphin's eMMC host controller and eMMC devices operating at speeds up to 400 MB/s.

The solution includes a PHY DFE control block as soft IP for configuration interface, and an AFE control block (hard macros of DLL and IO block). Compensation control and compensation pads are provided for automatic driver and receiver (ODT) termination impedance calibration.

eMMC/SD/SDIO - CONTROLLER (SOFT IP)

Dolphin's eMMC5.1/SD4.1/SDIO4.1 Controller is designed to quickly and easily integrate into any SoC, and is optimized to provide a complete solution when combined with Dolphin's PHY IP.

The Controller supports embedded MultiMediaCard, Secure Digital and Secure Digital I/O cards on any SoC. Connection between the application processor and the Controller is through industry-standard AMBA APB2 and AXI4. In addition, a DMA interface is also supported for data transfer.

	16nm FF+ FFC	28nm HP, HPx LP, ULP	40nm G, LP ULP	55nm GP, LP ULP, EF	65nm GP LP
Compliant with eMMC 5.1, SD 4.1 and SDIO 4.1 Specifications	●	●	●	●	●
Transfers data in HS400, HS200, DDR52, SDR52 compatibility modes	●	●	●	●	●
Supports HS400, HS200, DDR52 and SDR52 data transfer modes	●	●	●	●	●
Supports UHS-II (SD 4.0) data transfer rates up to 312MB/s	●	●	●	●	●
Supports UHS-I (SD 3.01) data transfer rates up to 104MB/s	●	●	●	●	●
Supports 32-bit and 64-bit system data bus and addressing	●	●	●	●	●
Tuning for HS200 mode	●	●	●	●	●
4KB block support	●	●	●	●	●
32 bit DMA interface	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●
Supports both Asynchronous and Synchronous AXI4 Interface	●	●	●	●	●
AXI4 Narrow Transfer	●	●	●	●	●
Enhanced strobe function for reliable operation at HS400 mode.	●	●	●	●	●
Host clock rate variable between 0 and 200 MHz	●	●	●	●	●
Transfers the data in 1-bit, 4-bit and 8-bit modes	●	●	●	●	●
Supports Low-Power mode	●	●	●	●	●
Supports CUP/Wirebond and Flip Chip configurations	●	●	●	●	●
Precision master/slave digital DLL is used for timing circuits.	●	●	●	●	●
PHY uses 6 metal layers. Higher metals are configurable for improved power and ground mesh	●	●	●	●	●
PHY includes built-in DLL (50-200 MHz) to handle high-speed operations	●	●	●	●	●
IDDQ Model	●	●	●	●	●
PVT compensation	●	●	●	●	●
Power supplies include Core VDD, I/O VDD and VSS	●	●	●	●	●
No use of deep n-well devices	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●

Front End views are available under NDA. For more information, contact: sales@dolphin-ic.com

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